CLAIMS

What is claimed is:

1. A stacked capacitor comprising:

a first capacitor having a first plate comprising a first semiconductive body and a second plate comprising a first floating electrode; and

a second capacitor having a first plate comprising a second semiconductive body and a second plate comprising a second floating electrode, the first and second semiconductive bodies being electrically isolated from each other, the first and second floating electrodes being connected together at an intercapacitor node.

2. The stacked capacitor of claim 1, wherein the first and second floating electrodes are only electrically connected to each other and to the intercapacitor node.

3. The stacked capacitor of claim 1, wherein additional circuit elements are electrically connected to the intercapacitor node, each of the additional circuit elements chosen from a group consisting of: a capacitor, a resistor, a diode, a field-effect transistor, a NFET, a PFET, a MOSCAP, a bipolar-junction transistor, a metal-semiconductor field-effect transistor, a FinFET, a vertical-gate transistor and an insulated-gate transistor.

4. The stacked capacitor of claim 1, wherein the first and second floating electrodes comprise a material chosen from a group consisting of: polysilicon, semiconductor material and a metal.

5. The stacked capacitor of claim 1, wherein the first and second semiconductive bodies comprise doped silicon.

6. The stacked capacitor of claim 1, wherein the intercapacitor node is configured to self-adjust to a value less than a working voltage impressed on the stacked capacitor.

7. The stacked capacitor of claim 1, wherein the intercapacitor node is configured to store a voltage when electrical power is removed from the stacked capacitor.

8. The stacked capacitor of claim 1, further comprising:

a charge injector coupled to the first and second floating electrodes; and

a charge drain coupled to the first and second floating electrodes, wherein the charge injector and charge drain are configured to adjust a floating voltage of the first and second floating electrodes to a value less than a working voltage of the stacked high-voltage capacitor.

9. The stacked capacitor of claim 1, wherein the stacked capacitor is formed on a substrate chosen from a group consisting of: bulk monocrystalline silicon, silicon on insulator and silicon on sapphire.

10. The stacked capacitor of claim 1, wherein the first and second capacitors each comprise at least one structure chosen from a group consisting of: PMOS-type and NMOS-type structures.

11. The stacked capacitor of claim 1, wherein at least the first capacitor comprises a PMOS-type structure and at least the first semiconductive body comprises an n-well.

12. The stacked capacitor of claim 1, wherein at least the first capacitor comprises a MOS capacitor.

13. The stacked capacitor of claim 1, wherein the first and second semiconductive bodies are formed on a semiconductor substrate having a first conductivity type and the first and second semiconductive bodies comprise wells of semiconductor material doped to have a second conductivity type opposite the first conductivity type, the wells being configured to be electrically isolated from

the semiconductor substrate and each other by one or more reverse-biased p-n junctions.

14. The stacked capacitor of claim 1, wherein at least the first capacitor comprises a tunneling dielectric disposed between the first and second plates.

15. The stacked capacitor of claim 1, wherein at least the first capacitor comprises a tunneling dielectric disposed between the first and second plates, and wherein the tunneling dielectric comprises materials chosen from a group consisting of: silicon dioxide, nitrided oxide, nitride, oxide/nitride composition, titanium oxide, tantalum oxide, zirconium oxide, hafnium oxide, lanthanum oxide, any lanthanide oxide, titanium silicate, tantalum silicate, zirconium silicate, hafnium silicate, lanthanum silicate and any lanthanide silicate.

16. The stacked capacitor of claim 1, wherein one of the first and second capacitors is a PMOS-type capacitor and another of the first and second capacitors is a NMOS-type capacitor.

17. The stacked capacitor of claim 1, wherein the first and second semiconductive bodies have a first conductivity type.

18. The stacked capacitor of claim 1, wherein the first and second semiconductive bodies have different conductivity types.

19. A stacked capacitor comprising a first capacitor and a second capacitor each including a first plate, a second plate and a tunneling dielectric disposed between the first and second plates, the first plates each being coupled to a respective terminal of the stacked capacitor, the second plates comprising a conductive layer forming floating electrodes and an intercapacitor node.

20. The stacked capacitor of claim 19, wherein at least one of the first plates comprises n-wells formed in a p-type substrate.

21. The stacked capacitor of claim 19, wherein at least one of the first plates comprises p-wells formed in an n-type substrate

22. The stacked capacitor of claim 19, wherein the first plates each comprise doped semiconductor regions formed in an insulating substrate.

23. The stacked capacitor of claim 19, wherein at least one of the second plates comprises a p-doped polysilicon common electrode.

24. The stacked capacitor of claim 19, wherein at least one of the second plates comprises an n-doped polysilicon common electrode.

25 The stacked capacitor of claim 19, wherein at least one of the second plates comprises an undoped polysilicon electrode.

26. The stacked capacitor of claim 19, wherein at least one of the second plates comprises a metal common electrode.

27. The stacked capacitor of claim 19, wherein the second plates are configured to self-adjust a voltage of the intercapacitor node to a value less than a working voltage of the stacked capacitor.

28. The stacked capacitor of claim 19, wherein:

the second plates are disposed atop the tunneling dielectric layer and each second plate is disposed over a respective first plate, the tunneling dielectric layer having a thickness of between 2 and 50 nanometers; and

the first plates each comprise a semiconductive body, the first plates each being electrically isolated from each other.

29. The stacked capacitor of claim 19, wherein the first and second capacitors each comprise PFET-type structures.

30. The stacked capacitor of claim 19, wherein the first and second capacitors each comprise NFET-type structures.

31. The stacked capacitor of claim 19, wherein the first and second capacitors each comprise a mix of PFET- and/or NFET-type structures.

32. A high-voltage stacked capacitor comprising a first capacitor and a second capacitor each including a first plate comprising a first semiconductive body and a second plate comprising a floating electrode, the first and second semiconductive bodies being electrically isolated from each other, the floating electrode including an intercapacitor node configured to self-adjust to a value less than a working voltage impressed on the stacked capacitor.

33. The high-voltage stacked capacitor of claim 32, wherein the first and second capacitors comprise FET-type structures formed on a substrate chosen from a group consisting of: silicon, glass, sapphire and insulative material.

34. The high-voltage stacked capacitor of claim 32, wherein the first and second capacitors are formed on a p-type silicon substrate, the first plates each comprise n-wells formed in the substrate and the floating electrode comprises polysilicon separated from the substrate by a tunneling dielectric comprising silicon dioxide.

35. The high-voltage stacked capacitor of claim 32, wherein the first and second capacitors are formed on an n-type silicon substrate, the first plates each comprise p-wells formed in the substrate and the floating electrode comprises polysilicon separated from the substrate by a tunneling dielectric comprising silicon dioxide.

36. The high-voltage stacked capacitor of claim 32, wherein the first capacitor comprises an NFET-type structure and the second capacitor comprises a PFET-type structure.

37. The high-voltage stacked capacitor of claim 32, wherein the first and second capacitors comprise MOS-type capacitors.

38. The high-voltage stacked capacitor of claim 32, wherein at least one of the first and second capacitors includes a tunneling dielectric separating the first and second plates.

39. The high-voltage stacked capacitor of claim 32, wherein at least one of the first and second capacitors operates in an inversion mode.

40. The high-voltage stacked capacitor of claim 32, wherein at least one of the first and second capacitors operates in an accumulation mode.

41. The high-voltage stacked capacitor of claim 32, wherein at least one of the first and second capacitors is an MOS-type capacitor and operates in an accumulation mode.

42. The high-voltage stacked capacitor of claim 32, wherein at least one of the first and second capacitors is an MOS-type capacitor and operates in an inversion mode.

43. A high-voltage stacked capacitor comprising:

a substrate; and

first and second capacitors each comprising:

an n-well formed in the substrate and comprising an electrode of the high-voltage stacked capacitor, each n-well being isolated from the substrate;

a tunneling dielectric disposed atop each of the n-wells; and

a floating electrode comprising polysilicon disposed on the tunneling dielectric atop at least a portion of each of the n-wells and extending therebetween.

44. The high-voltage stacked capacitor of claim 43, wherein the tunneling dielectric has a thickness of between 1 nm and 50 nm.

45. The high-voltage stacked capacitor of claim 43, wherein the tunneling dielectric comprises silicon dioxide.

46. The high-voltage stacked capacitor of claim 43, wherein the floating electrode is configured to self-adjust to a floating voltage whose value is less than a working voltage of the high-voltage stacked capacitor and is configured to store the floating voltage when electrical power is removed from the high-voltage stacked capacitor.

47. The high-voltage stacked capacitor of claim 43, further comprising:

a charge injector coupled to the floating electrode; and

a charge drain coupled to the floating electrode, wherein the charge injector and charge drain are configured to adjust a floating voltage of the floating electrode to a value less than a working voltage of the stacked high-voltage capacitor.

48. The high-voltage stacked capacitor of claim 43, wherein at least one of the n-wells includes an n+ contact.

49. The high-voltage stacked capacitor of claim 43, wherein at least one of the first and second capacitors is configured to operate in an inversion mode.

50. The high-voltage stacked capacitor of claim 43, wherein at least one of the first and second capacitors is configured to operate in an accumulation mode.

51. The high-voltage stacked capacitor of claim 43, wherein at least one of the n-wells includes a p+ implant.

52. The high-voltage stacked capacitor of claim 43, wherein the substrate comprises a p-type silicon substrate.

53. A high-voltage stacked capacitor comprising:

a substrate; and

first and second capacitors each comprising:

a semiconductive well supported by the substrate and comprising an electrode of the high-voltage stacked capacitor, each well being electrically isolated from the substrate and from each other;

a tunneling dielectric disposed atop each of the wells; and

a floating electrode comprising polysilicon disposed on the tunneling dielectric atop at least a portion of each of the wells and extending therebetween.

54. The high-voltage stacked capacitor of claim 53, wherein the tunneling dielectric has a thickness of between 1 nm and 50 nm.

55. The high-voltage stacked capacitor of claim 53, wherein the tunneling dielectric comprises silicon dioxide.

56. The high-voltage stacked capacitor of claim 53, wherein the floating electrode is configured to self-adjust to a floating voltage whose value is less than a working voltage of the high-voltage stacked capacitor.

57. The high-voltage stacked capacitor of claim 53, further comprising:

a charge injector coupled to the floating electrode; and

a charge drain coupled to the floating electrode, wherein the charge injector and charge drain are configured to adjust a floating voltage of the floating electrode to a value less than a working voltage of the stacked high-voltage capacitor.

58. The high-voltage stacked capacitor of claim 53, wherein the floating electrode is configured to store a floating voltage when electrical power is removed from the high-voltage stacked capacitor.

59. The high-voltage stacked capacitor of claim 53, wherein at least one of the wells comprises an n-well.

60. The high-voltage stacked capacitor of claim 53, wherein at least one of the wells includes an n+ contact.

61. The high-voltage stacked capacitor of claim 53, wherein at least one of the wells comprises a p-well.

62. The high-voltage stacked capacitor of claim 53, wherein at least one of the wells includes a p+ contact.

63. The high-voltage stacked capacitor of claim 53, wherein at least one of the first and second capacitors is configured to operate in an inversion mode.

64. The high-voltage stacked capacitor of claim 53, wherein at least one of the first and second capacitors is configured to operate in an accumulation mode.

65. The high-voltage stacked capacitor of claim 53, wherein the substrate comprises p-type silicon.

66. The high-voltage stacked capacitor of claim 53, wherein the substrate comprises n-type silicon.

67. A high-voltage stacked capacitor comprising:

first and second capacitor means sharing a common floating electrode; and

charge injection and extraction means coupled to the first and second capacitor means and configured to set a voltage of the common floating electrode to a value less than a working voltage of the high-voltage stacked capacitor.

68. The high-voltage stacked capacitor of claim 67, wherein the first and second capacitor means comprise FET-type structures.

69. The high-voltage stacked capacitor of claim 67, wherein the first and second capacitor means comprise MOS-type capacitor structures.

70. The high-voltage stacked capacitor of claim 67, wherein the first and second capacitor means comprise bodies of semiconductive material that are electrically isolated from each other.

71. The high-voltage stacked capacitor of claim 67, wherein the charge injection and extraction means comprises a tunneling oxide disposed adjacent the common floating electrode.

72. The high-voltage stacked capacitor of claim 67, wherein the common floating electrode comprises polysilicon.

73. The high-voltage stacked capacitor of claim 67, wherein the first and second capacitor means comprise bodies of semiconductive material that are electrically isolated from each other, the charge injection and extraction means

comprises a tunneling oxide disposed between each of the bodies of semiconductive material and the common floating electrode, and wherein the common floating electrode comprises polysilicon.

74. The high-voltage stacked capacitor of claim 67, wherein the charge injection and extraction means comprise:

a charge injector coupled to the floating electrode; and

a charge drain coupled to the floating electrode, wherein the charge injector and charge drain are configured to adjust the voltage of the common floating electrode.

75. The high-voltage stacked capacitor of claim 67, wherein the floating electrode is configured to store the voltage on the common floating electrode when electrical power is removed from the high-voltage stacked capacitor.

76. A process for charging a floating electrode of a high-voltage stacked capacitor, comprising:

coupling a first potential to a first electrode of the high-voltage stacked capacitor, the first electrode being coupled to a first semiconductive body;

coupling a second potential to a second electrode of the high-voltage stacked capacitor, the second electrode being coupled to a second semiconductive

body that is electrically isolated from the first semiconductive body, a difference between the first and second potentials comprising a working voltage of the high-voltage stacked capacitor; and

charging a floating electrode to a floating voltage whose value is less than the working voltage, wherein the floating electrode is capacitively coupled to the first and second semiconductive bodies and includes an intercapacitor node.

77. The process of claim 76, further comprising storing the floating voltage on the floating electrode following removal of the first and second potentials from the high-voltage stacked capacitor.

78. The process of claim 76, wherein the act of charging comprises tunneling charge carriers through a dielectric, wherein the dielectric includes a first portion disposed between the first semiconductive body and a corresponding portion of the floating electrode and the dielectric includes a second portion disposed between the second semiconductive body and a corresponding portion of the floating electrode.

79. The process of claim 76, wherein the acts of coupling first and second potentials comprise coupling the first and second potentials to first and second electrodes of the high-voltage stacked capacitor, and wherein the high-

voltage stacked capacitor comprises a plurality of PFETs, NFETs or MOSCAPs, or any combination thereof coupled to the common intercapacitor node.